**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (Original) A method for computing compressed serial scan-in values for a scan-chain, said method comprising:

beginning with a desired scan-chain state as an initial current scan-chain state, said desired scan-chain state comprising one or more care-in values and zero or more don't-care values, repeatedly computing a previous scan-chain state and serial scan-in input value that must have existed one shift cycle prior to said current scan-chain state and setting said previous scan-chain state as the said current scan-chain state, until said current scan-chain state has pre-determined values in pre-determined bit positions of said scan-chain; and

forming said compressed serial scan-in values from said computed serial scan-in input values.

2. (Original) A method as described in claim 1, wherein said compressed serial scan-in input values are generated using a data spreading network that receives a multiplicity of external serial input values that are used to generate a greater number of said serial scan-in input values than said multiplicity of external serial input values.

3. (Original) A method as described in claim 1, where said scan-chain comprises a multiplicity of scan-chain segments, wherein inserting serial data into said scan-chain segments is performed by combining a next bit value of said serial scan-in input and a multiplicity of present values of scan-chain bit positions previous to the first bit positions of said scan-chain segments.

4. (Original) A method as described in claim 3, wherein said compressed serial scan-in input

values are generated using a data spreading network that receives a multiplicity of external serial input values that are used to generate a greater number of said serial scan-in input values than said multiplicity of external serial input values.

5. (Original) A method of testing an integrated circuit comprising at least one scan-chain, at least one said scan-chain comprising a multiplicity of scan-chain segments, said method comprising:

loading at least one of said at least one scan chain using compressed serial scan-in values determined according to the method of Claim 4.

6. (Original) A method as described in claim 1, wherein said forming comprises:

taking said computed serial scan-in input values in reverse order.

7. (Original) A method of testing an integrated circuit that contains scan-chains using compressed scan-chain patterns, wherein at least one of said compressed scan-chain patterns is computed according to the method of Claim 1.

8. (Original) A method to compute compressed sequences of values for decompression by a data spreading network,said method comprising:

starting with sequences of don't care and care-in values desired to be produced by said data-spreading network, applying successive values from said sequences of don't care and care-in values to the outputs of said data spreading network;

resolving values on the inputs of said data spreading network associated with said outputs of said data spreading network, to produce resolved values; and

forming said compressed sequences of values as compressed sequences from said resolved values.

9. (Original) A method as in claim 8, wherein said resolving values on the inputs of said data spreading network comprises:

generating one or more symbolic expressions associated with said inputs, said one or more symbolic expressions being formed as functions of input variables and said successive values applied to the outputs of said data spreading network; and

resolving values of said input variables and said one or more symbolic expressions.

10. (Original) A method as in claim 8, wherein said resolving values on the inputs of said data spreading network comprises:

generating one or more symbolic expressions associated with said inputs and a set of one or more state variables that represent an internal state of said data spreading network, said one or more symbolic expressions being formed as functions of one or more of the following: input variables; said successive values applied to the outputs of said data spreading network; and present values of said one or more state variables;

replacing present values of said one or more state variables with symbolic expressions associated with said one or more state variables; and

resolving values of said input variables and said symbolic expressions.

11. (Original) A method for loading a scan-chain, said scan-chain comprising a multiplicity of scan-chain segments, said method comprising:

inserting pseudo-random serial data into at least one of said scan-chain segments, said inserting including applying a combination of a next bit value of said pseudo-random serial input data and a multiplicity of values of scan bit positions previous to first bit positions of said scan-chain segments.

12. (Original) A method of testing an integrated circuit comprising at least one scan-chain, at least one of said at least one scan-chain comprising a multiplicity of scan-chain segments, said

method comprising:

loading at least one of said at least one scan chain according to the method of Claim 11.

13. (Original) A scan flip-flop, comprising;

a Scan_In port;

a Data_In port;

a Scan_Enable port;

a CLK port;

a Data_Out port;

and having a means to:

capture data from said Data_In port in one state of a signal on said Scan Enable port by applying a change to signal on said CLK port thereby changing it to a pre-defined CLK state;

capture data from said Scan_In port in a different state of the signal on said Scan_Enable port by applying said change to signal on said CLK port thereby changing it to said pre-defined CLK state;

disable loading data from either of said Scan_In port and said Data_In port in said pre-defined state of signal on said CLK port; and

use a combination of states of signals on said Scan_Enable port and said CLK port to enable reflecting said captured data at said Data_Out port, said reflected data on said Data_Out port being held constant at other times.

14. (Original) A circuit structure comprising:

a multiplicity of scan-chains, wherein at least one of said scan-chains comprises a multiplicity of flip-flops as described in claim 13, at least one said Scan_Enable port of at least one said flip-flop being coupled to a control signal wherein:

in one state, said control signal provides information to select operation of said flip-flop responsive to said Scan_In port or responsive to said Data_In port; and

in another state, said control signal provides information to select operation of said flip-flop to reflect said captured data at its Data_Out port.

15. (Original) A method of distributing a control signal for a scan-chain that receives a clock signal having at least two states, the method comprising:

using said control signal to carry information to select operation of said scan-chain between a system mode of operation and a scan mode of operation when said clock signal is in a first state;

using said control signal to carry information to select between updating said scan-chain with new data values and leaving present data values in said scan-chain unchanged when said clock signal is in a second state.

16. (Original) A structure for controlling a multiplicity of clocks, comprising:

a control input;

a count input; and

a common clock, wherein said structure enables the said common clock to generate each of the multiplicity of clocks individually;

wherein the structure implements a mode to enable all the multiplicity of clocks in one state of said control input and a mode to successively enable each one of the multiplicity of clocks in one state of the count input.

17. (Original) A circuit structure as in claim 16, further comprising:

a data input; and

a multiplicity of scan chains, each clocked by one of said multiplicity of clocks;

wherein a multiplicity of data values from said data input is successively scanned into each one of said multiplicity of scan chains, one scan chain at a time.

18. (Original) An integrated circuit (IC), comprising:

a multiplicity of mode-control signals, each adapted to assume one of at least two states;

a multiplicity of scan-chains, each comprising at least one flip-flop;

a multiplicity of blocking circuits, each of said multiplicity of blocking circuits receiving at least one data-in signal and adapted to be responsive to at least one said mode-control signal, each of said multiplicity of blocking circuits providing serial scan data to at least one flip-flop of said multiplicity of scan-chains;

wherein each of said blocking circuits outputs a value that is representative of a combination of a value on said at least one data-in signal of said blocking circuit and at least one value of at least one scan bit position previous to said at least one flip-flop, in at least a first state of said multiplicity of mode control inputs;

and

each of said blocking circuits outputs a constant value, in at least a second state of said multiplicity of mode control inputs.

19. (Original) The integrated circuit according to Claim 18, further comprising:

a multiplicity of multi-input signature register (MISR) blocks that are adapted to be responsive to a multiplicity of outputs of said multiplicity of blocking circuits.

20. (Original) The integrated circuit according to Claim 18, wherein each of said blocking circuits comprises:

a multiplexer adapted to be responsive to at least one said mode-control signal;

a logic gate adapted to be coupled to a first data input of said multiplexer, said logic gate adapted to receive as inputs at least one data-in signal and at least one additional input from a scan bit position previous to said at least one flip-flop.

21. (Currently Amended) The integrated circuit according to Claim 20 ~~21~~, wherein said at

least one additional input from a scan position previous to said at least one flip-flop is coupled to at least a second data input of said multiplexer; and

wherein said multiplexer is adapted to produce an output value that is representative of a signal value at said first data input in a first state of said mode-control signal; and

wherein said multiplexer is adapted to produce an output value that is representative of signal value at said at least a second data input in a second mode of said mode-control signal.

22. (Original) The integrated circuit according to Claim 18, further comprising:

a multiplicity of multi-input signature register (MISR) blocks, wherein each of said MISR blocks is prevented from capturing "X" states from a multiplicity of tap points on said scan chain when one or more of said tap points contain said "X" state.

23. (Original) An apparatus for eliminating "X" states within a scan chain, the apparatus comprising:

one or more blocking circuits adapted to selectively replace propagated states with known states when one or more of said "X" states are propagated from one flip-flop of said scan chain to a next flip-flop of said scan chain through said blocking circuits.

24. (Original) A boundary scan flip-flop comprising:

a data-in port;

a data-out port;

a scan-in port;

a scan-out port;

a probe-in port;

a probe-out port;

a test port; and

a flip-flop;

wherein said ports and said flip-flop are adapted to implement at least:

a system operation mode, enabled by one state of said test port, wherein said boundary scan flip-flop propagates a signal from said data-in port to said data-out port, and selects between propagating a signal from said probe-in port and said data-in port based on a state of said flip-flop; and

a test operation mode, enabled by a different state of said test port, wherein said boundary scan flip-flop propagates a signal from said probe-in port to said probe-out port, and captures a signal on said data-in port for shifting out through said scan-in and scan-out ports.

25. (Original) The boundary scan flip-flop as in Claim 24, further comprising:

a first multiplexer adapted to be coupled to said data-in port and to said flip-flop, an output of said first multiplexer adapted to be coupled to said data-out port, the first multiplexer adapted to be responsive to a signal from said test port; and

a second multiplexer adapted to be coupled to said probe-in port and to said data-in port, an output of the second multiplexer adapted to be coupled to said probe-out port, the second multiplexer adapted to be responsive so said signal from said test port.

26. (Original) The boundary scan flip-flop as in Claim 25, further comprising:

a logic gate coupled to said flip-flop and to said test port, an output of said logic gate adapted to provide a select input to said second multiplexer.

27. (Original) A multiplicity of boundary scan flip-flops as in claim 24, connected to form a multiplicity of boundary scan chains, wherein at least one of said boundary scan-chains contains a multiplicity of scan segments such that any data in port of any boundary scan flip-flop may be probed during system operation.

28. (Original) A multiplicity of boundary scan flip-flops as in claim 27, wherein at least one

compressed test pattern is used during said test operation mode.

29. (Original) An integrated circuit (IC), comprising:

a multiplicity of primary serial inputs; and

a multiplicity of scan-chains;

wherein at least one of said multiplicity of scan-chains comprises multiple scan-chain segments, each of said multiple scan-chain segments having a segment serial input, wherein said segment serial inputs to a multiplicity of subsequent ones of said multiple scan-chain segments are determined as at least one function of said primary serial inputs combined with a multiplicity of scan positions of a multiplicity of previous ones of said multiple scan-chain segments.

30. (Original) A machine-readable medium that provides instructions that, when executed by a computing platform, cause said computing platform to perform operations comprising the method according to Claim 1.

31. (Original) A machine-readable medium that provides instructions that, when executed by a computing platform, cause said computing platform to perform operations comprising the method according to Claim 8.